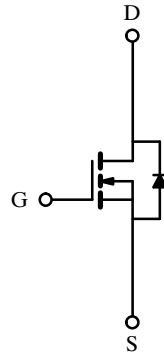
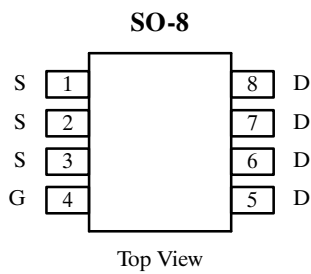


N-Channel Enhancement-Mode MOSFET

Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
30	0.0135 @ $V_{GS} = 10$ V	± 10
	0.020 @ $V_{GS} = 4.5$ V	± 8



N-Channel MOSFET

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	$T_A = 25^\circ\text{C}$	± 10
		$T_A = 70^\circ\text{C}$	± 8
Pulsed Drain Current	I_{DM}	± 50	A
Continuous Source Current (Diode Conduction) ^a	I_S	2.3	
Maximum Power Dissipation ^a	P_D	$T_A = 25^\circ\text{C}$	2.5
		$T_A = 70^\circ\text{C}$	1.6
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	50	$^\circ\text{C}/\text{W}$

Notes

a. Surface Mounted on FR4 Board, $t \leq 10$ sec.

Subsequent updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #1230.

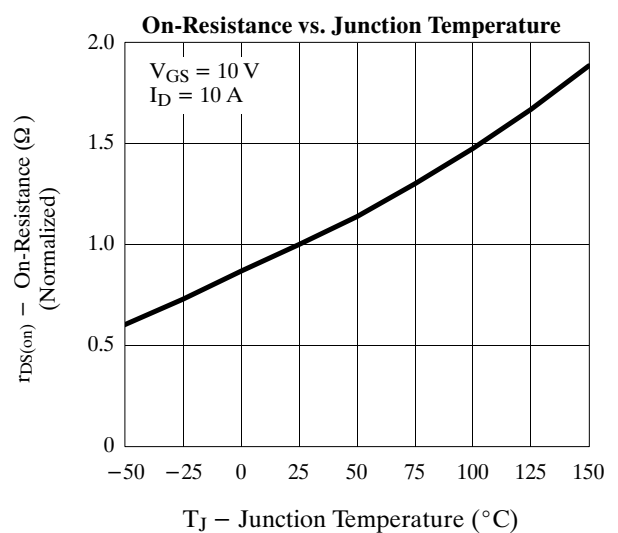
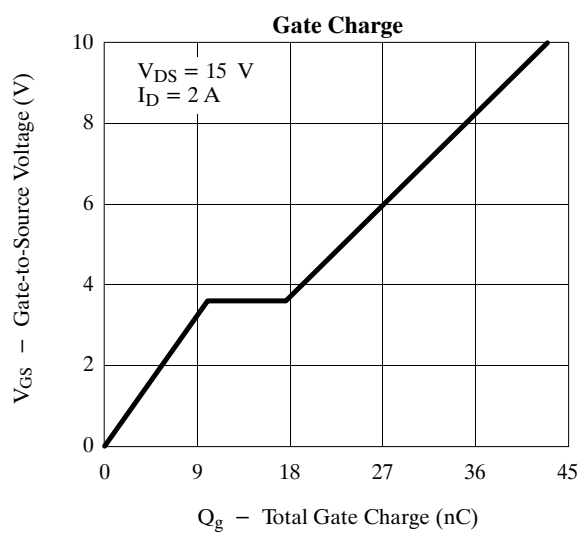
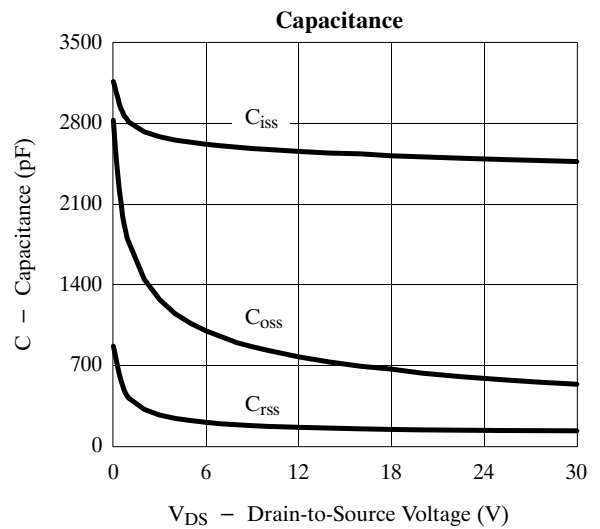
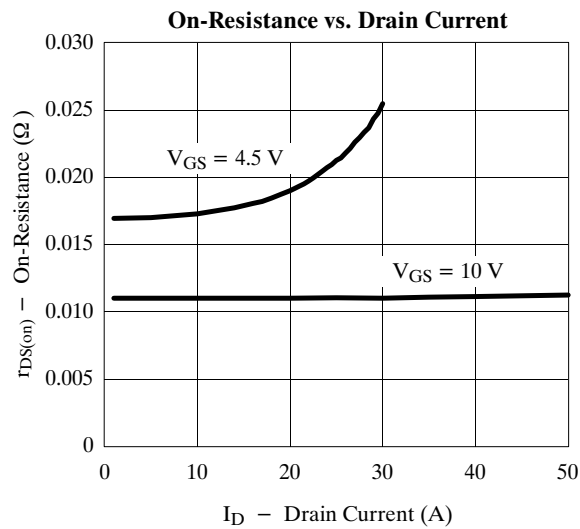
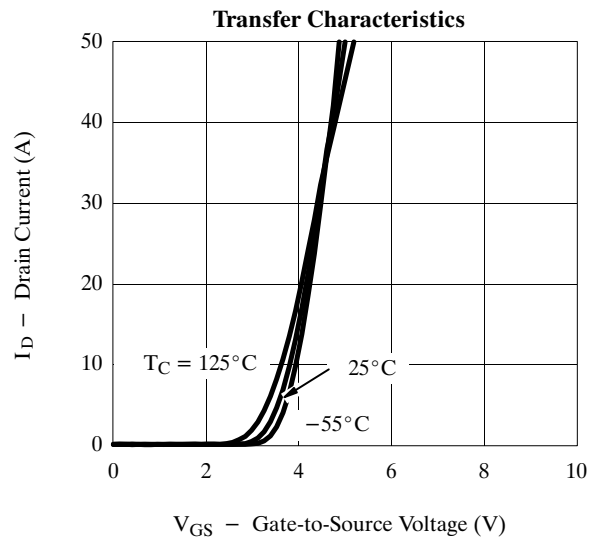
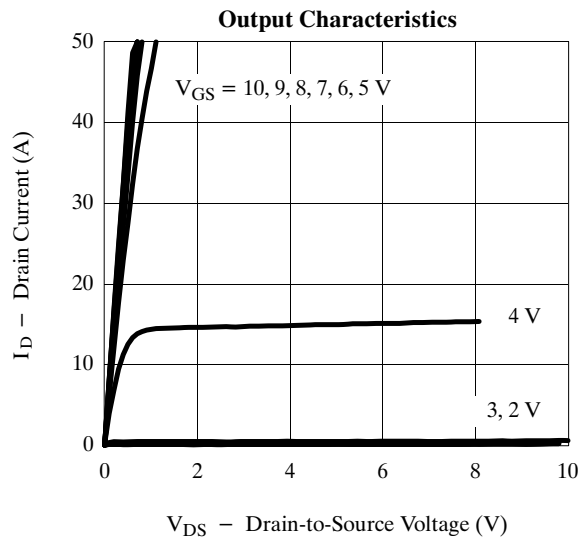
Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ ^a	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	1.0			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}, T_J = 55^\circ\text{C}$			25	
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	20			A
Drain-Source On-State Resistance ^b	$r_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 10\text{ A}$		0.011	0.0135	Ω
		$V_{GS} = 4.5\text{ V}, I_D = 5\text{ A}$		0.0165	0.020	
Forward Transconductance ^b	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 10\text{ A}$		19		S
Diode Forward Voltage ^b	V_{SD}	$I_S = 2.3\text{ A}, V_{GS} = 0\text{ V}$		0.75	1.1	V
Dynamic^a						
Total Gate Charge	Q_g	$V_{DS} = 15\text{ V}, V_{GS} = 10\text{ V}, I_D = 2\text{ A}$		43	60	nC
Gate-Source Charge	Q_{gs}			10		
Gate-Drain Charge	Q_{gd}			7.5		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 25\text{ V}, R_L = 25\ \Omega$ $I_D \cong 1\text{ A}, V_{GEN} = 10\text{ V}, R_G = 6\ \Omega$		17	30	ns
Rise Time	t_r			11	20	
Turn-Off Delay Time	$t_{d(off)}$			60	100	
Fall Time	t_f			45	80	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 2.3\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		55	80	

Notes

- a. Guaranteed by design, not subject to production testing.
- b. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

Typical Characteristics (25°C Unless Otherwise Noted)



Si4410DY

Typical Characteristics (25°C Unless Otherwise Noted)

